Xiaoxiao LIANG

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Education

Hong Kong University of Science and Technology (Guangzhou) 2022 – 2026

Ph.D. in Microelectronics, supervised by Prof. Yuzhe MA

Hong Kong University of Science and Technology 2020 – 2021

M.S. in Electronic Engineering, supervised by Prof. Xiaomeng LI

Huazhong University of Science and Technology 2016 – 2020

B.Eng. in Automation

Work Experience

Shenzhen GWX Technology, SMIT Mar. 2024 – Feb. 2025

Research Intern

Source-mask optimization for VLSI fabrication

Hong Kong University of Science and Technology (Guangzhou) Jan. 2022 – Jul. 2022

Research Assistant Advisor: Prof. Yuzhe MA

Photomask optimization for VLSI fabrication

Hong Kong University of Science and Technology Jul. 2021 – Dec. 2021

Research Assistant Advisor: Prof. Xiaomeng LI

Privacy-preserving federated framework building for medical image analysis

Publications

Xiaoxiao Liang, Yang Luo, Bei Yu, Yuzhe Ma, “BEAM: Bidirectional MEEF-Driven Mask Optimization for Photonic Integrated Circuits”. *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2026.

Xiaoxiao Liang, Benjamin C. He, Yuzhe Ma, “A Diffusion Model-enhanced Source Optimization for Fab Productivity”. *SPIE Optics + Photonics*, 2025.

Xiaoxiao Liang, Haoyu Yang, Kang Liu, Bei Yu, Yuzhe Ma, “CAMO: Correlation-Aware Mask Optimization with Modulated Reinforcement Learning”. *Design Automation Conference (DAC)*, 2024.

Xiaoxiao Liang, Yikang Ouyang, Haoyu Yang, Bei Yu, Yuzhe Ma, “RL-OPC: Mask Optimization With Deep Reinforcement Learning”. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2024.

Xiaoxiao Liang, Yiqun Lin, Huazhu Fu, Lei Zhu, Xiaomeng Li, “RSCFed: Random Sampling Consensus Federated Semi-supervised Learning”. *IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, 2022.

Ziyang Yu, Shuo Yin, Su Zheng, **Xiaoxiao Liang**, Yuzhe Ma, Bei Yu, “Coordinated Clip-Wise Gradient Scheduling for Full-Chip ILT via Policy Learning”. *Design Automation Conference (DAC)*, 2026.

Su Zheng, **Xiaoxiao Liang**, Ziyang Yu, Yuzhe Ma, Bei Yu, Martin Wong, “Curvilinear Optical Proximity Correction via Cardinal Spline”. *Design Automation Conference (DAC)*, 2025.

Minjie Bi, Yang Luo, **Xiaoxiao Liang**, Zhengzhou Gu, Jinbin Deng, Binwu Zhu, Yuzhe Ma, “Efficient SRAF Generation via Diffusion Models”. *International Symposium of EDA*, 2025.

Yang Luo, **Xiaoxiao Liang**, Yuzhe Ma, “Enabling Robust Inverse Lithography with Rigorous Multi-Objective Optimization”, *International Conference on Computer-Aided Design (ICCAD)*, 2024.

Ziyang Yu, Su Zheng, Wenqian Zhao, Shuo Yin, **Xiaoxiao Liang**, Guojin Chen, Yuzhe Ma, Bei Yu, Martin DF Wong, “RuleLearner: OPC Rule Extraction From Inverse Lithography Technique Engine”. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, 2024.

PATENTS

梁潇潇, 马宇哲, “掩模版校正方法、装置、计算机设备及可读存储介质”, 中国国家发明专利, 专利号: ZL 2024 1 1005241.5, 公开号: CN 118781028 B, 授权日期: 2025-12-16.

梁潇潇, 马宇哲, “一项面向曲线型光芯片版图的掩模优化技术”, 中国国家发明专利实质审查阶段, 公开号: CN 121411063 A, 公开日期: 2026-01-27.

马宇哲, **梁潇潇**, 欧阳奕康, “一种光学临近效应校正方法、系统、设备及存储介质”, 中国国家发明专利实质审查阶段, 公开号: CN 117192888 A, 公开日期: 2023-12-21.

NOTABLE PROJECTS

Lithography Mask Optimization for Photonic IC Designs

Jan. 2025 – Present

- Developed a novel mask optimization method targeting curvilinear PIC layouts in photonic chip fabrication
- Built a customized optimization framework with efficient curvilinear layout and mask representations
- Designed a white-box optimization algorithm leveraging a surrogate model for EPE sensitivity, enabling flexible corrections with reduced computational cost
- Efficiently produces manufacturing-friendly photomasks with high fidelity

Latent Diffusion Pipeline for Accelerated Lithography Source Optimization

Apr. 2024 – Feb. 2025

- Developed a diffusion-based framework for advanced-node photolithography source optimization
- Built a user-friendly latent diffusion pipeline conditioned on layout and process parameters
- Designed a batching and superposition strategy to handle complex layouts
- Efficiently generated high-quality source initializations, accelerating SMO workflows.

Reinforcement Learning-based Lithography Mask Optimization for VLSI Fabrication

Jan. 2022 – Present

- Developed advanced OPC techniques at the layout level for VLSI manufacturing
- Introduced RL for automated OPC, enabling efficient layout pattern transferring
- Customized intelligent agent to efficiently capture layout spatial correlations and accelerate convergence
- Led the workflow of layout data collection with EDA tools, framework design, and implementation
- Published two first-authored papers in top-tier EDA venues including *TCAD'24* and *DAC'24*

HONORS AND AWARDS

ICCAD Student Scholar Program Grant	2024
DAC Young Student Fellow	2024
Full Postgraduate Scholarship, HKUST(GZ)	2022-2026
Excellent Student Scholarship, HKUST	2021
Outstanding Graduate, HUST	2020
Academic Scholarship, HUST	2016-2017

SKILLS

- Languages
  English, Chinese
- Programming Language
  Python, C/C++
- Deep Learning Framework
  PyTorch, TensorFlow
- EDA Tools
  Calibre, Innovus